Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-8 (canceled).

Claim 9 (currently amended): In a microprocessor-based computing system having a CPU for executing tasks represented by task register sets and further including peripheral devices that issue interrupt commands, an interrupt and task change processing circuit comprising:
(a) a task enable circuit for determining from predetermined inputs whether a predetermined task is ready for execution by the central processing unit,
(b) a task priority selection circuit coupled to an output of the task enable circuit for determining an order for the running of tasks that have been determined ready for execution by the task enable circuit; and
(c) a task switching circuit coupled to an output of the task priority selection circuit for controlling the execution of tasks in a sequence determined by the task priority selection circuit, ~~The interrupt and task change processing circuit of claim 4~~ wherein the task switching circuit is coupled to a zero overhead multiplexing circuit for storing a later task in a first set of latches during a first clock cycle while simultaneously switching a previously stored earlier task stored in a second set of latches into a task switch controller during the same clock cycle.

Claim 10 (original): In a microprocessor-based computing system having a CPU for executing tasks represented by task register sets and further including peripheral devices that issue interrupt commands, the combination comprising: (a) an interrupt and task change processing circuit for responding to interrupt commands and for placing tasks in an order of priority for execution by the CPU, and (b) a zero overhead multiplexing circuit coupled to the interrupt and task change processing circuit for storing a later task in a first set of latches during a first clock cycle while

simultaneously switching a previously stored earlier task stored in a second set of latches into a memory unit during the same clock cycle.

Claim 11 (original): The combination of claim 10 wherein the interrupt and task change processing circuit includes a task enable circuit for placing a task in a status in which it is ready for execution by the CPU.

Claim 12 (original): The combination of claim 11 wherein the interrupt and task change processing circuit includes a task priority selection circuit for assigning a task priority to tasks which are ready for execution by the CPU.

Claim 13 (original): The combination of claim 12 wherein the interrupt and task change processing circuit includes a task switching circuit for loading tasks ready for execution by the CPU into said zero overhead multiplexing circuit based upon their task priority.

Claims 14-16 (canceled).